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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,655	05/10/2005	Christian Reichinger	DE02 0249 US	6552
24738	7590	06/27/2006	EXAMINER ALMO, KHAREEM E	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			ART UNIT 2816	PAPER NUMBER

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/534,655	REICHINGER, CHRISTIAN
	Examiner Khareem E. Almo	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 10 May 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-7 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 10 May 2005 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>5/10/2005</u> .	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other: _____.
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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (US 4291274).

With respect to claim 1, Figure 2 of Suzuki et al. discloses a phase comparator, for a PLL module, that compares the phase angle of a first input signal (SIG) with a second input signal (REF) by evaluating the edges of the input signals and generates reset signals (R) therefrom, characterized in that at least one additional circuit (10, and 11) is provided that evaluates further, different edges of the input signal or signals and generates therefrom additional reset signals (R) for the regulating signal or signals.

With respect to claim 2, Figure 2 of Suzuki et al. discloses a phase comparator as claimed in claim 1, characterized in that the phase comparator obtains the regulating signals from the rising/decaying edges of the input signals and in that the additional circuit derives the additional reset signals from the decaying/rising edges of the input signals.

With respect to claim 3, Figure 2 of Suzuki et al. discloses a phase comparator as claimed in claim 1, characterized in that a dedicated additional circuit is provided for each of the two input signals (REF and SIG), with one additional circuit (10) evaluating

the edges of the first input signal (REF) and the second additional circuit (11) evaluating the edges of the second input signal (SIG).

With respect to claim 4, Figure 2 of Suzuki et al. discloses a phase comparator as claimed in claim 1, characterized in that one additional circuit (10 and 11) evaluates the rising and decaying edges of one input signal (REF) and the other additional circuit evaluates the rising and decaying edges of the other input signal (SIG).

With respect to claim 5, Figure 2 of Suzuki et al. discloses a phase comparator as claimed in claim 1, characterized in that the output signals from the additional circuits (10, 11 and 12) are applied to the reset inputs of flip-flops (8 and 9) belonging to the phase comparator via a gate (12), there also being connected to the gate a gate (and gates to 8 and 9) to which the regulating signals are applied.

With respect to claim 6, Figure 2 of discloses a phase comparator as claimed in claim 1, characterized in that the additional circuits each have two RS flip-flops and gates (10 and 11), which are integrated into the PLL circuit.

With respect to claim 7, Figure 16 of Suzuki et al. discloses a phase comparator that compares the phase angle of a first input signal (SIG) with a second input signal (REF) by evaluating the edges of the input signals and generates reset signals therefrom, characterized in that at least one additional circuit (27 and 29) is provided that evaluates further, different edges of the input signal or signals and generates therefrom additional reset signals for the regulating signal or signals characterized in that the two input signals (SIG and REF) are applied to the additional circuit via an OR gate (from 28 and 30).

3. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsinker (US 6323692).

With respect to claim 1, Figure 10 of Tsinker discloses a phase comparator, for a PLL module, that compares the phase angle of a first input signal (FILTER CLOCK) with a second input signal (REF. CLOCK) by evaluating the edges of the input signals and generates reset signals (RESET_DN and RESET_UP) therefrom, characterized in that at least one additional circuit (202) is provided that evaluates further, different edges of the input signal or signals and generates therefrom additional reset signals (UPDN_RST) for the regulating signal or signals.

With respect to claim 2, Figure 10 of Tsinker discloses a phase comparator as claimed in claim 1, characterized in that the phase comparator obtains the regulating signals from the rising/decaying edges of the input signals and in that the additional circuit derives the additional reset signals (UPDN_RST) from the decaying/rising edges of the input signals.

With respect to claim 3, Figure 10 of Tsinker discloses a phase comparator as claimed in claim 1, characterized in that a dedicated additional circuit (202 and 204) is provided for each of the two input signals (REF CLOCK and FILTER CLOCK), with one additional circuit (204) evaluating the edges of the first input signal (REF CLOCK) and the second additional circuit (202) evaluating the edges of the second input signal (FILTER CLOCK).

With respect to claim 4, Figure 10 of Tsinker discloses a phase comparator as

claimed in claim 1, characterized in that one additional circuit (202) evaluates the rising and decaying edges of one input signal (FILTER CLOCK) and the other additional circuit (204) evaluates the rising and decaying edges of the other input signal (REF CLOCK).

With respect to claim 5, Figure 10 of Tsinker discloses a phase comparator as claimed in claim 1, characterized in that the output signals (DN and UP) from the additional circuits (204 and 202) are applied to the reset inputs(RN) of flip-flops belonging to the phase comparator via a gate (216 and 218), there also being connected to the gate a gate (212 and 214) to which the regulating signals are applied.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


KEA
6/21/06


Quan Tra
Primary Examiner